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10/738,407	12/16/2003	Muthu Venkatachalam	Intel-008PUS	8314

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EXAMINER	
SOL, ANTHONY M	

ART UNIT	PAPER NUMBER
2619	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/738,407	VENKATACHALAM ET AL.	
	Examiner	Art Unit	
	ANTHONY SOL	2619	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 January 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *27-41* is/are allowed.

6)☒ Claim(s) *1,3-16,18-26 and 42-45* is/are rejected.

7)☒ Claim(s) *17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

- Applicant's Amendment filed 1/7/2008 is acknowledged.
- Objections to claims 9, 43, and 45 are withdrawn.
- Claims 9, 43, and 45 have been amended.
- Claims 1 and 3-45 remain pending.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 3-16, 18-26, and 42-45 are rejected under 35 U.S.C. 102(e) as being anticipated by Pub. No. US 2004/0213255 A1 ("Brinkerhoff").

Regarding claims 1,

Brinkerhoff shows in fig. 7 a first multi-threaded processor engine 74 configured for connection to a serial link HSSI (para. 91, line 11)

Brinkerhoff further shows in fig. 7, second multi-threaded processor

engine 62A that includes multiple processors 63 , coupled to the first multi-threaded processor engine by an interface 68, to process data received by the first multi-threaded processor over the serial link and to provide the processed data to the first multi-threaded processor engine for transmission over the serial link (para.89-91).

Brinkerhoff discloses one or more communication data structures usable by the first and second multi-threaded processor engines to control interaction therebetween (para. 53, *According to a specific embodiment, when a given line card is electrically coupled to the system 60 of FIG. 7, the respective* ***line rates*** *of the ports residing on that line card may be stored in line card memory 72. This* ***data*** *may then be* ***accessed by a processor such as 62A or 62B****, which uses the port line rate information to calculate a* ***respective cell interval value*** *for each port. The cell interval values may then be stored locally in memory such as, for example, in CPU memory 61 or in system memory 65. Since data from each client flow is associated with a respective port, the cell interval value associated with a particular client flow may be equal to the cell interval rate for the associated port, adjusted by any QoS parameter(s) associated with that client flow (if desired). Once the cell interval value for a specific client flow has been determined, that value may be stored in Table 650, which may reside, for example, in processor memory or system memory (FIG. 7))*(also see paras. 50-52 and 54 and table 650 of fig. 6A for a full description of cell interval values and how they are dynamically calculated so that a client flow may be equal to the cell interval rate for the associated port),

Brinkerhoff further discloses wherein at least one of the one or more communication data structures is usable by the first and second multi-threaded processor engines to control the rate at which the processed data is provided to the first multi-threaded processor engine by the second multi-threaded engine (para. 104, *a scheduler 806, which may be configured to shape the output from system 800 by controlling the* ***rate*** *at which data leaves an output port*; para. 126, ***Scheduler 806 uses information from processor 816*** *which provides specific scheduling instructions and other information to be used by the scheduler for generating one or more output data streams*; para. 127, *Scheduler 806 may also be configured to synchronize output data from switching logic 810 to the various output ports, for example, to prevent overbooking of output ports*).

Regarding claim 3,

Brinkerhoff discloses a Frame Relay interface (para. 93).

Regarding claim 4,

Brinkerhoff discloses HDLC data (para. 118).

Regarding claims 5 and 6,

Brinkerhoff discloses ATM data (para. 118).

Regarding claim 7,

Brinkerhoff discloses interworking logic 802 that convert frames to ATM cells and vice versa (claimed Inverse Multiplexing for ATM)(para. 121).

Regarding claim 8,

Brinkerhoff discloses HDLC frames and ATM cells (paras. 118, 121).

Regarding claim 9,

Brinkerhoff shows in fig. 7, a TDM 67B where several data streams of lower data rate is combined into one data stream of a higher data rate.

Regarding claims 10, 12, and 25,

Brinkerhoff discloses memory arbiter configured to handle the timing and execution of data access operations requested by various system components (para. 127).

Regarding clam 11,

Brinkerhoff discloses storing channel number and port number identifiers (para. 119).

Regarding claims 13, 14, and 16,

Brinkerhoff discloses a scheduler 806 that may be configured to synchronize output data from switching logic 810 to various output ports, for example to prevent overbooking of output ports and also manage memory 808 access requests from various system components in fig. 7 and 8 (para. 127).

Regarding claim 15,

Brinkerhoff discloses that the respective line rates of the ports residing on that line card may be stored in line card memory 72. This data may then be accessed by a processor such as 62A or 62B, which uses the port line rate information to calculate a respective cell interval value for each port. The **cell interval values** may then be stored locally in memory such as, for example, in CPU **memory 61 or in system memory 65**. Since data from each client flow is associated with a respective port, the cell interval value associated with a particular client flow may be equal to the cell interval rate for the associated port, adjusted by any QoS parameter(s) associated with that client flow (if desired). Once the cell interval value for a specific client flow has been determined, that value may be stored in Table 650, which may reside, for example, in processor memory or system memory (FIG. 7))(also see paras. 50-52 and 54 and table 650 of fig. 6A for a full description of cell interval values and how they are dynamically calculated so that a client flow may be equal to the cell interval rate for the associated port and transmitted over line 309).

Regarding claim 18,

Brinkerhoff discloses a Table 650 of fig. 6A containing cell interval value which represents how often a data packet from a particular flow is to be transmitted over line 309 (para. 50). Brinkerhoff further discloses that cell interval values may be stored in CPU memory 61 of second multi-threaded processor engine 62A or in system memory

65 (para. 53). Brinkerhoff still further discloses **retrieving** cell interval values N_i (claimed polling) and parameter T, which may be represented as an integer which keeps track of the total number of ATM cells which have been transmitted over line 309 since the start of the Preemptive Bandwidth Procedure (para. 59) and **comparing** the values of N1, N2, and N3 with value T in order to determine whether each of these values exceeds the value of T.

Regarding claim 19,

Brinkerhoff shows in fig. 2, FIFO buffers 202A and 202B and transceiver buffer 212. Brinkerhoff discloses ports configured to handle ATM cells (para.118).

Regarding claim 20,

Brinkerhoff discloses that system 800 operates in various formats including Frame Relay and ATM (para. 118).

Regarding claims 21-23,

Brinkerhoff discloses that as data is received at serial ports, it is initially processed by protocol conversion and parsing logic 804 and is determined where bytes and frames/cells start and end. Brinkerhoff further discloses that data from memory 808 is then classified as either ATM or Frame Relay (paras. 119, 120).

Regarding claim 24,

Brinkerhoff discloses that line cards 70 performs functions such as encryption and other functions (claimed co-processor)(para. 97).

Regarding claim 26,

Brinkerhoff discloses that the serial link can be T1, E1, Ethernet or Frame Relay (para. 93).

Regarding claim 42,

Brinkerhoff shows in fig. 7 a first multi-threaded processor engine 74 configured for connection to a serial link HSSI (para. 91, line 11)

Brinkerhoff further shows in fig. 7, second multi-threaded processor engine 62A that includes multiple processors 63 , coupled to the first multi-threaded processor engine by an interface 68, to process data received by the first multi-threaded processor over the serial link and to provide the processed data to the first multi-threaded processor engine for transmission over the serial link (para.89-91).

Brinkerhoff discloses one or more communication data structures usable by the first and second multi-threaded processor engines to control interaction therebetween (para. 53, *According to a specific embodiment, when a given line card is electrically coupled to the system 60 of FIG. 7, the respective* ***line rates*** *of the ports residing on that line card may be stored in line card memory 72. This* ***data*** *may then be* ***accessed by a processor such as 62A or 62B****, which uses*

the port line rate information to calculate a ***respective cell interval value*** *for each port. The cell interval values may then be stored locally in memory such as, for example, in CPU memory 61 or in system memory 65. Since data from each client flow is associated with a respective port, the cell interval value associated with a particular client flow may be equal to the cell interval rate for the associated port, adjusted by any QoS parameter(s) associated with that client flow (if desired). Once the cell interval value for a specific client flow has been determined, that value may be stored in Table 650, which may reside, for example, in processor memory or system memory (FIG. 7))*(also see paras. 50-52 and 54 and table 650 of fig. 6A for a full description of cell interval values and how they are dynamically calculated so that a client flow may be equal to the cell interval rate for the associated port),

Brinkerhoff further discloses wherein at least one of the one or more communication data structures is usable by the first and second multi-threaded processor engines to control the rate at which the processed data is provided to the first multi-threaded processor engine by the second multi-threaded engine (para. 104, *a scheduler 806, which may be configured to shape the output from system 800 by controlling the* ***rate*** *at which data leaves an output port*; para. 126, ***Scheduler 806 uses information from processor 816*** *which provides specific scheduling instructions and other information to be used by the scheduler for generating one or more output data streams*; para. 127, *Scheduler 806 may also be configured to synchronize output data*

from switching logic 810 to the various output ports, for example, to prevent overbooking of output ports).

Brinkerhoff discloses one or more communication data structures usable by the first and second multi-threaded processor engines to control interaction therebetween (para. 53, *According to a specific embodiment, when a given line card is electrically coupled to the system 60 of FIG. 7, the respective* ***line rates*** *of the ports residing on that line card may be stored in line card memory 72. This* ***data*** *may then be* ***accessed by a processor such as 62A or 62B****, which uses the port line rate information to calculate a* ***respective cell interval value*** *for each port. The cell interval values may then be stored locally in memory such as, for example, in CPU memory 61 or in system memory 65. Since data from each client flow is associated with a respective port, the cell interval value associated with a particular client flow may be equal to the cell interval rate for the associated port, adjusted by any QoS parameter(s) associated with that client flow (if desired). Once the cell interval value for a specific client flow has been determined, that value may be stored in Table 650, which may reside, for example, in processor memory or system memory (FIG. 7))*(also see paras. 50-52 and 54 and table 650 of fig. 6A for a full description of cell interval values and how they are dynamically calculated so that a client flow may be equal to the cell interval rate for the associated port),

Brinkerhoff further discloses wherein at least one of the one or more communication data structures is usable by the first and second multi-threaded

processor engines to control the rate at which the processed data is provided to the first multi-threaded processor engine by the second multi-threaded engine (para. 104, *a scheduler 806, which may be configured to shape the output from system 800 by controlling the* ***rate*** *at which data leaves an output port*; para. 126, ***Scheduler 806 uses information from processor 816*** *which provides specific scheduling instructions and other information to be used by the scheduler for generating one or more output data streams*; para. 127, *Scheduler 806 may also be configured to synchronize output data from switching logic 810 to the various output ports, for example, to prevent overbooking of output ports*).

Brinkerhoff discloses that the respective line rates of the ports residing on that line card may be stored in line card memory 72. This data may then be accessed by a processor such as 62A or 62B, which uses the port line rate information to calculate a respective cell interval value for each port. The **cell interval values** may then be stored locally in memory such as, for example, in CPU **memory 61 or in system memory 65**. Since data from each client flow is associated with a respective port, the cell interval value associated with a particular client flow may be equal to the cell interval rate for the associated port, adjusted by any QoS parameter(s) associated with that client flow (if desired). Once the cell interval value for a specific client flow has been determined, that value may be stored in Table 650, which may reside, for example, in processor memory or system memory (FIG. 7))(also see paras. 50-52 and 54 and table 650 of fig. 6A for a full description of cell interval values and how they are

dynamically calculated so that a client flow may be equal to the cell interval rate for the associated port and transmitted over line 309).

Brinkerhoff discloses a Table 650 of fig. 6A containing cell interval value which represents how often a data packet from a particular flow is to be transmitted over line 309 (para. 50). Brinkerhoff further discloses that cell interval values may be stored in CPU memory 61 of second multi-threaded processor engine 62A or in system memory 65 (para. 53). Brinkerhoff still further discloses **retrieving** cell interval values N_i (claimed polling) and parameter T, which may be represented as an integer which keeps track of the total number of ATM cells which have been transmitted over line 309 since the start of the Preemptive Bandwidth Procedure (para. 59) and **comparing** the values of N1, N2, and N3 with value T in order to determine whether each of these values exceeds the value of T.

Regarding claim 43,

Brinkerhoff discloses a scheduler 806 that controls the rate at which data leaves an output port (para. 104).

Regarding claim 44,

Brinkerhoff shows in fig. 7, a first multi-threaded processor engine 74,

Brinkerhoff further shows in fig. 7, a second multi-threaded processor engine 62A that includes multiple processors 63 operable to process data received from a network via a network interface 68.

Brinkerhoff discloses that the first multi-threaded processor engine is configured to operate as a co-processor for the second multi-threaded processor engine (para. 97, Brinkerhoff discloses that line cards 70 performs functions such as encryption and other functions (claimed co-processor)).

Brinkerhoff further discloses that the co-processor 74 performs hardware accelerator task such as data parcel switching, media control and management, framing, interworking, protocol conversion, data parsing, etc. (para. 91).

Regarding claim 45,

Brinkerhoff discloses one connection may include a CPU interface that allows configuration data to be sent from CPU 62B to configuration registers on selected line cards 70 (para. 98). Brinkerhoff further discloses memory arbiter configured to handle the timing and execution of data access operations requested by various system components (para. 127).

Response to Arguments

3. Applicant's arguments filed 1/7/2008 have been fully considered but they are not persuasive.

- The Applicant argues beginning on bottom of pg. 17 that Brinkerhoff does not disclose or suggest that at least one of the one or more communication data structures is usable by the first and second multi-threaded processor engines to control the rate at which the processed

data is provided to the first multi-threaded processor engines by the second multi-threaded engine.

- The Examiner respectfully disagrees. The 3rd paragraph of the rejection to claim 1 discusses the limitation aforementioned and is reproduced below:

> Brinkerhoff discloses one or more communication data structures usable by the first and second multi-threaded processor engines to control interaction therebetween (para. 53, *According to a specific embodiment, when a given line card is electrically coupled to the system 60 of FIG. 7, the respective* ***line rates*** *of the ports residing on that line card may be stored in line card memory 72. This* ***data*** *may then be* ***accessed by a processor such as 62A or 62B****, which uses the port line rate information to calculate a* ***respective cell interval value*** *for each port. The cell interval values may then be stored locally in memory such as, for example, in CPU memory 61 or in system memory 65. Since data from each client flow is associated with a respective port, the cell interval value associated with a particular client flow may be equal to the cell interval rate for the associated port, adjusted by any QoS parameter(s) associated with that client flow (if desired). Once the cell interval value for a specific client flow has been determined, that value may be stored in Table 650, which may reside, for example, in processor memory or system memory (FIG. 7)*)(also see paras. 50-52 and 54 and table 650 of fig. 6A for a full description of cell interval values and how they are dynamically calculated so that a9 client flow may be equal to the cell interval rate for the associated port),

In other words, when a line card is electrically coupled, such as when it is plugged/swapped in to a physical slot of the switch, the line rates of the ports along with other parameters are determined between the CPU and the processor of the line card, and the line rate data is stored in line card memory 72, which may then be accessed by a processor such as 62A or 62B, which **uses the port line rate information to calculate a respective cell interval value for each port**. The cell interval values may then be stored locally in memory such as, for example, in CPU memory 61 or in system memory 65. Since data from each client flow is associated with a respective port, the cell interval value associated with a particular client flow may be equal to the **cell interval rate for the associated port**

- The Applicant further argues on pg. 18 that the Examiner has failed to provide support in Brinkerhoff that line card processor 74 nor CPU 62A is a multithreaded processor. The Applicant further argues that the Examiner had indicated that in the first Office action that Brinkerhoff indicates that CPU 62A is a MIPS and that the Applicant had requested that the Examiner provide support that MIPS is a multithreaded processor, which the Office action mailed 10/18/2007 does not provide.
- The Examiner in the Office action mailed 10/18/2007 omitted any mention of MIPS. Thus, this argument is moot. However, the Examiner does not

concede that MIPS is not a "multithreaded" processor and will provide appropriate support if necessary as the prosecution warrants. In response to applicant's argument that line card processor 74 and CPU 62A are not "multithreaded" processors, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In other words, since the claim does not recite any positive functional limitations associated with "multithreading" that the prior art (Brinkerhoff) is not capable of performing, then Brinkerhoff does meet the claim.

- The Applicant still further argues on pg. 19 that the Examiner erroneously indicated that the line card processor 74 uses the scheduler 806 and submits that processor 816 is not a line card processor 74, and thus, line card processor does not use system 800. Thus, the Applicant argues that Brinkerhoff never discloses or suggests that the **processor 62A and processor 74 use the scheduler 804** to control the rate at which the processed data is provided to the processor 74 by the processor 62A. Therefore, Brinkerhoff does not disclose or suggest that at least one of the one or more communication data structures is usable by the first and second multi-threaded processor engines to control the rate at which the

processed data is provided to the first multi-threaded processor engine by the second multi-threaded engine.

- The Examiner respectfully disagrees. The Office action never indicated that the line card processor 74 uses the scheduler 806. The relevant portion of the rejection of claim 1 dealing with the above limitation is reproduced below:

> Brinkerhoff further discloses wherein at least one of the one or more communication data structures is usable by the first and second multi-threaded processor engines to control the rate at which the processed data is provided to the first multi-threaded processor engine by the second multi-threaded engine (para. 104, *a scheduler 806, which may be configured to shape the output from system 800 by controlling the* ***rate*** *at which data leaves an output port*; para. 126, ***Scheduler 806 uses information from processor 816*** *which provides specific scheduling instructions and other information to be used by the scheduler for generating one or more output data streams*; para. 127, *Scheduler 806 may also be configured to synchronize output data from switching logic 810 to the various output ports, for example, to prevent overbooking of output ports*).

It is clear from the above that there is no mention of line card processor 74 using the scheduler 806. In fact, line card processor 74 is not mentioned

at all. It does say that the scheduler 806 may be configured to shape the output from system 800 by controlling the rate at which data leaves an output port, but it does not say that scheduler 806 is in the line card processor 74. As for the contention that Brinkerhoff never discloses or suggests that the processor 62A and processor 74 **use the scheduler 804** to control the rate at which the processed data is provided to the processor 74 by the processor 62A, it is noted that the feature upon which applicant relies (i.e., that processor 62A and processor 74 **use the scheduler 804** to control the rate at which the processed data is provided to the processor 74 by the processor 62A) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). In other words, scheduler 804 is not recited in the claim. The claim recites a "data structure," which a scheduler is not. A "data structure" has already been mapped in the rejection of claim 1 and discussed above in response to the first argument, as line card memory 72. It should be noted that the scheduler does use cell interval value of table 650 which was calculated by the processor 62A or 62B (claimed second multi-threaded engine) based on the line rates of the ports residing on the line cards and stored in line card memory 72 (claimed data structure) as determined by the CPU and the processor of the line card (claimed first multi-threaded engine)

and then accessed by a processor such as 62A or 62B as explained in detail to the first argument above, thus the data structure is usable by the first multithreaded processor engine to control the rate at which the processed data is provided to the first multithreaded processor engine by the second multi-threaded engine.

- The Applicant still further argues on pg. 21 that claim 42 includes corresponding features to claims 27, 34, and 38 (which have been allowed) and that the Brinkerhoff reference should be withdrawn.
- The Examiner respectfully disagrees that clam 42 includes corresponding features of claims 27, 34, and 38. Claim 42 is much broader than claims 27, 34, and 38.

- The Applicant still further argues on pg. 22 regarding claim 44 that Brinkerhoff refers to the interface 68 and not the co-processor 74 in arguing that Brinkerhoff does not disclose or suggest using the multi-threaded physical layer network processor engine as a co-processor to perform a hardware accelerator task associated with the multi-threaded packed processing.
- The Examiner respectfully disagrees. Brinkerhoff discloses that interfaces 68 may be implemented as **interface cards, also referred to as line cards** (para. 91). And as it is clear from fig. 7, line card 70 includes

processor 74 (claimed co-processor). Therefore, co-processor 74 performs hardware accelerator tasks.

Allowable Subject Matter

4. Claims 27-41 are allowed.

Claim 17 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim **and any intervening claims**.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ANTHONY SOL whose telephone number is (571)272-5949. The examiner can normally be reached on M-F 7:30am - 4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wing Chan can be reached on (571) 272-7493. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/A. S./
Examiner, Art Unit 2619
4/8/2008

/Wing F Chan/
Supervisory Patent Examiner, Art Unit 2619
3/31/08